UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,212	02/05/2004	Hsin-Huang Hsieh	17620R-003200US	6912

20350 7590 05/03/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,212	HSIEH ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election made on January 18, 2005.

Election/Restrictions

Applicant's election of Group I, claims 1-15 in the reply filed on January 18, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Peake et al. (US Pub. 2004/0188775 A1).

In re claim 6, Peake et al. shows (fig. 13) shows a semiconductor device set which comprises at least two types of devices (11 and 11e), each of the two types of devices having a trench feature (20 and 20e); wherein the first device (11) comprises a gate oxide (17) formed in the trench feature, a polysilicon layer (11) formed on the gate

oxide in the trench features, a first isolation layer (18) formed on the polysilicon layer and having an opening, and a metal layer (23) formed on the first isolation layer and filling the opening of the first isolation layer; and wherein the second device (11e) comprises a dielectric layer (51e) formed adjacent an opening at a top of the trench feature on opposite sides of the trench feature, a gate oxide (17) formed in the trench feature and over the dielectric layer, a polysilicon layer (11e) formed on the gate oxide in the trench feature including a space near the top of the trench feature with the dielectric layer disposed on opposite sides thereof, a second isolation (18e) layer formed on the dielectric layer, and a metal layer (110 g) formed on the polysilicon layer.

In re claim 7, Peak discloses [0034-0035] that the at least two types of devices are formed on a silicon substrate.

In re claim 8, Peak discloses [0034-0035] the silicon substrate has an epitaxial layer (14) formed thereon.

In re claim 9, Peake shows (fig. 13) that the epitaxial layer has a P substrate thereon (150 or 15 (p)).

In re claim 10, Peake shows (fig. 13) that each trench feature (20e or 20) extends through the P substrate to an area below a top surface of the epitaxial layer (14).

In re claim 11, Peake shows (fig. 13) that a plurality of N source regions (13) and a plurality of P regions (35) are formed in the P substrate.

In re claim 12, Peak shows (fig. 2) the complete device in which at least two of the N source regions (13) found in the P substrate are disposed adjacent to and on

opposites sides of one of the first devices, and wherein at least one of the P regions (35) formed in the P substrate is disposed between two adjacent N source regions.

In re claim 13, Peake shows (fig. 13) that the epitaxial layer (14) is an N epitaxial layer.

In re claim 14, Peake discloses [0034-0035] that the silicon substrate is an N substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peake et al. (US Pub. 2004/0188775 A1) as applied to claim 6 above.

In re claim 15, Peake does not specifically disclose that the dielectric layer in the second device is a field oxide layer. However, it is well known in the art that the nitride mask layer of Peake could be substituted with oxide to also provide an isolation function. One of ordinary skill knows that an oxide instead of nitride may provide a specific etch selectivity, a specific dielectric constant, or reduction in process steps since the device is already configured to be oxidized in certain portions of the device. Furthermore, the designation of "field" for the oxide layer merely recites an intended use of a known material, i.e. a thick oxide. The thick dielectric of Peake adjacent the trench

will also provide a field isolation function. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the nitride layer of Peake by using an oxide as is well known in the art to provide isolation with a specific dielectric constant or to form the dielectric without additional processing steps.

Allowable Subject Matter

Claims 1-5 are allowed.

The following is an examiner's statement of reasons for allowance: In re claim 1, the prior art references, alone or in combination do not show a trenched DMOS device formed atop an N+ silicon substrate with an N epitaxial layer thereon including a device region and a bus region neighboring the device region, the bus region comprising: a field oxide formed on the P substrate and a bus trench extending down from a top surface of the field oxide; a gate oxide layer formed in the bus trench and extending to cover a top surface of the P substrate; and a polysilicon bus formed in the bus trench and having a top surface disposed at a lower level than the top surface of the field oxide layer. The closes reference, Williams et al. (US 6,413,822 B2) shows (fig. 23) a bus region (270) comprising a nitride layer (274) formed on a P substrate, a bus trench extending down from a top surface of the nitride, and a polysilicon bus (272) formed in the bus trench and having a top surface disposed at a level higher than the top surface of the nitride layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Williams et al. (6,413,822 B2), Yilmaz et al. (US 5,597,765), and Blanchard et al. (US 4,791,462) also show DMOS trench devices having gate bus or termination regions formed in a trench.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
April 28, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER